

## Claims

We Claim:

1 1. A method of designing an electrical wiring structure having a plurality of wires, said method  
2 comprising identifying at least one wire pair, said wire pair including a first wire of the plurality  
3 of wires and a second wire of the plurality of wires, said second wire already tri-stated or can be  
4 tri-stated, said wire pair having a same-direction switching probability  $\phi_{SD}$  per clock cycle that is  
5 no less than a pre-selected minimum same-direction switching probability  $\phi_{SD,MIN}$  or having an  
6 opposite-direction switching probability  $\phi_{OD}$  per clock cycle that is no less than a pre-selected  
7 minimum opposite-direction switching probability  $\phi_{OD,MIN}$ , said first wire and said second wire  
8 satisfying at least one mathematical relationship, said at least one mathematical relationship  
9 involving  $L_{COMMON}$  and  $W_{SPACING}$ , said  $W_{SPACING}$  defined as a spacing between the first wire and  
10 the second wire, said  $L_{COMMON}$  defined as a common run length of the first wire and the second  
11 wire.

1 2. The method of claim 1, said at least one mathematical relationship comprising:

2  $W_{SPACING}$  no greater than a pre-selected minimum spacing  $W_{SPACING, MAX}$ ; and

3  $L_{COMMON}$  no less than a pre-selected minimum common run length  $L_{COMMON, MIN}$ .

1 3. The method of claim 1, said at least one mathematical relationship comprising  $F_{LW} \geq F_{LW,MIN}$ ,  
2 said  $F_{LW}$  defined as  $L_{COMMON}/W_{SPACING}$ , said  $F_{LW,MIN}$  defined as a pre-selected minimum value of  
3  $F_{LW}$ .

1 4. The method of claim 1, wherein identifying at least one wire pair comprises:

2 identifying at least one high-power wire; and

3 for a high-power wire of the at least one high-power wire, identifying a good neighbor  
4 wire of the high-power wire, wherein the first wire of the wire pair is the high-power wire, and  
5 wherein the second wire of the wire pair is the good neighbor wire.

1 5. The method of claim 1, wherein said second wire is not already tri-stated but can be tri-stated,  
2 and further comprising adding tri-stating logic to the second wire.

1 6. The method of claim 1, wherein  $\phi_{OD}$  is no less than  $\phi_{OD,MIN}$ , and further comprising adding  
2 logic for inverting the second wire along the common run length.

1 7. The method of claim 1, further comprising adding blocking logic for blocking propagation of a  
2 signal from the second wire while the second wire is tri-stated.

1 8. The method of claim 1, further comprising reducing  $W_{\text{SPACING}}$ .

1 9. The method of claim 1, wherein the at least one wire pair includes a plurality of wire pairs, and  
2 further comprising:

3 ranking the wire pairs in accordance with power dissipation savings;

4 developing a list of the ranked wire pairs in sorted order of the power dissipation savings;

5 and

6 truncating the list at a point of diminishing returns in the power dissipation savings, in  
7 accordance with a predetermined truncation criterion.

10 10. The method of claim 1, wherein  $W_{\text{SPACING}}$  is a predetermined spacing, and wherein  $L_{\text{COMMON}}$  is  
2 a predetermined common run length.

11 11. The method of claim 1, wherein  $W_{\text{SPACING}}$  is an established spacing, and wherein  $L_{\text{COMMON}}$  is  
2 an established common run length.

1 12. A method for executing a two-wire voltage transition, comprising the steps of:

2 providing two wires of an electrical wire network, said two wires denoted as an A wire  
3 and a B wire, said A wire having a capacitance  $C_A$ , said B wire having a capacitance  $C_B$ , said A  
4 wire and B wire having a coupling capacitance  $C_C$  between the A wire and the B wire;

5 tri-stating the B wire from a voltage  $V_{B1}$  to a high impedance state;

6 after tri-stating the B wire, transitioning the A wire from a voltage  $V_{A1}$  to a voltage  $V_{A2}$   
7 such that  $V_{A2} \neq V_{A1}$ ; and

8 after transitioning the A wire to  $V_{A2}$ , transitioning the B wire to a voltage  $V_{B2}$  such that  
9  $V_{B2} \neq V_{B1}$ .

10 13. The method of claim 12, wherein  $(V_{A2} - V_{A1})(V_{B2} - V_{B1}) > 0$ .

11 14. The method of claim 13, wherein the A wire and the B wire have a same-direction switching  
12 probability per clock cycle  $\phi_{SD}$  that is no less than a pre-selected minimum same-direction  
13 switching probability  $\phi_{SD,MIN}$ .

1 15. The method of claim 13, wherein  $V_{A1} = V_{B1} = 0$  and  $V_{A2} = V_{B2} = 1$ , and wherein an effective  
2 capacitance of the two-wire voltage transition is  $C_A + C_B$ .

1 16. The method of claim 13, wherein  $V_{A1} = V_{B1} = 1$  and  $V_{A2} = V_{B2} = 0$ , and wherein an effective  
2 capacitance of the two-wire voltage transition is 0.

1 17. The method of claim 12, wherein  $(V_{B2} - V_{B1})(V_{A2} - V_{A1}) < 0$ , wherein the A wire and the B wire  
2 have a common run length, and further comprising inverting the B wire along the common run  
3 length.

1 18. The method of claim 17, wherein the A wire and the B wire have an opposite-direction  
2 switching probability per clock cycle  $\phi_{OD}$  that is no less than a pre-selected minimum opposite-  
3 direction switching probability  $\phi_{OD,MIN}$ .

1 19. The method of claim 17, wherein  $V_{A1} = 0$ ,  $V_{B1} = 1$ ,  $V_{A2} = 1$ , and  $V_{B2} = 0$ , and wherein an  
2 effective capacitance of the two-wire voltage transition is  $C_A + C_B$ .

1 20. The method of claim 17, wherein  $V_{A1} = 1$ ,  $V_{B1} = 0$ ,  $V_{A2} = 0$ , and  $V_{B2} = 1$ , and wherein an  
2 effective capacitance of the two-wire voltage transition is 0.

1 21. The method of claim 12, further comprising blocking propagation of a signal from the B wire  
2 while the B wire is tri-stated.

1 22. An electrical wiring structure, comprising at least one wire pair, said wire pair including a  
2 first wire and a second wire, said second wire slated for being tri-stated, said wire pair having a  
3 same-direction switching probability  $\phi_{SD}$  per clock cycle that is no less than a pre-selected  
4 minimum same-direction switching probability  $\phi_{SD,MIN}$  or having an opposite-direction switching  
5 probability  $\phi_{OD}$  per clock cycle that is no less than a pre-selected minimum opposite-direction  
6 switching probability  $\phi_{OD,MIN}$ , said first wire and said second wire satisfying at least one  
7 mathematical relationship, said at least one mathematical relationship involving  $L_{COMMON}$  and  
8  $W_{SPACING}$ , said  $W_{SPACING}$  defined as a spacing between the first wire and the second wire, said  
9  $L_{COMMON}$  defined as a common run length of the first wire and the second wire.

10 23. The electrical wiring design of claim 22, said at least one mathematical relationship  
11 comprising:

12  $W_{SPACING}$  no greater than a pre-selected minimum spacing  $W_{SPACING,MAX}$ ; and

13  $L_{COMMON}$  no less than a pre-selected minimum common run length  $L_{COMMON,MIN}$ .

1 24. The electrical wiring design of claim 22, said at least one mathematical relationship  
2 comprising  $F_{LW} \geq F_{LW,MIN}$ , said  $F_{LW}$  defined as  $L_{COMMON}/W_{SPACING}$ , said  $F_{LW,MIN}$  defined as a pre-  
3 selected minimum value of  $F_{LW}$ .

1 25. The electrical wiring design of claim 22, wherein the first wire of the wire pair is a high-  
2 power wire, and wherein the second wire of the wire pair is a good neighbor wire of the high

3 power wire.

1 26. The electrical wiring design of claim 22, wherein  $\phi_{OD}$  is no less than  $\phi_{OD,MIN}$ , and further  
2 comprising logic for inverting the second wire along the common run length.

1 27. The electrical wiring design of claim 22, further comprising blocking logic for blocking  
2 propagation of a signal from the second wire while the second wire is tri-stated.

1 28. The electrical wiring design of claim 22, wherein  $W_{SPACING}$  is a predetermined spacing, and  
2 wherein  $L_{COMMON}$  is a predetermined common run length.

1 29. The electrical wiring design of claim 22, wherein  $W_{SPACING}$  is an established spacing, and  
2 wherein  $L_{COMMON}$  is an established common run length.

1 30. An electrical wire structure, comprising two wires of a wire network, said two wires denoted  
2 as an A wire and a B wire, said A wire having a capacitance  $C_A$ , said B wire having a capacitance  
3  $C_B$ , said A wire and B wire having a coupling capacitance  $C_C$  between the A wire and the B wire,  
4 said B wire in a tri-state, said A wire transitioning from a voltage  $V_{A1}$  to a voltage  $V_{A2}$  such that  
5  $V_{A2} \neq V_{A1}$ , said B wire having transitioned to the tri-state from a voltage  $V_{B1}$ , said B wire  
6 intended to be transitioned to a voltage  $V_{B2}$  such that  $V_{B2} \neq V_{B1}$  after the A wire has transitioned  
7 to the voltage  $V_{A2}$ , said transition of the A wire from the voltage  $V_{A1}$  to the voltage  $V_{A2}$  and of the  
8 B wire from the voltage  $V_{B1}$  to the voltage  $V_{B2}$  identified as a two-wire voltage transition.

1 31. The electrical wire network of claim 30, wherein  $(V_{A2} - V_{A1})(V_{B2} - V_{B1}) > 0$ .

1 32. The electrical wire network of claim 31, wherein the A wire and the B wire have a same-  
2 direction switching probability per clock cycle  $\phi_{SD}$  that is no less than a pre-selected minimum  
3 same-direction switching probability  $\phi_{SD,MIN}$ .

1 33. The electrical wire network of claim 31, wherein  $V_{A1} = V_{B1} = 0$  and  $V_{A2} = V_{B2} = 1$ , and  
2 wherein an effective capacitance of the two-wire voltage transition is  $C_A + C_B$ .

1 34. The electrical wire network of claim 31, wherein  $V_{A1} = V_{B1} = 1$  and  $V_{A2} = V_{B2} = 0$ , and  
2 wherein an effective capacitance of the two-wire voltage transition is 0.



1 35. The electrical wire network of claim 30, wherein  $(V_{B2} - V_{B1})(V_{A2} - V_{A1}) < 0$ , wherein the A wire  
2 and the B wire have a common run length, and further comprising the B wire inverted along the  
3 common run length.

1 36. The electrical wire network of claim 35, wherein the A wire and the B wire have an opposite-  
2 direction switching probability per clock cycle  $\phi_{OD}$  that is no less than a pre-selected minimum  
3 opposite-direction switching probability  $\phi_{OD,MIN}$ .

1 37. The electrical wire network of claim 35, wherein  $V_{A1} = 0$ ,  $V_{B1} = 1$ ,  $V_{A2} = 1$ , and  $V_{B2} = 0$ , and  
2 wherein an effective capacitance of the two-wire voltage transition is  $C_A + C_B$ .

1 38. The electrical wire network of claim 35, wherein  $V_{A1} = 1$ ,  $V_{B1} = 0$ ,  $V_{A2} = 0$ , and  $V_{B2} = 1$ , and  
2 wherein an effective capacitance of the two-wire voltage transition is 0.

1 39. The electrical wire network of claim 30, wherein propagation of a signal from the B wire  
2 while the B wire is being blocked.

1 40. A computer system for designing an electrical wiring structure having a plurality of wires,  
2 comprising:

3 a processor;

4 an input device coupled to the processor;

5 an output device coupled to the processor;

6 a first memory device coupled to the processor;

7 a second memory device coupled to the processor;

8 a computer code stored in the second memory device and executed by the processor; said  
9 computer code comprising an algorithm, said algorithm identifying at least one wire pair, said  
10 wire pair including a first wire of the plurality of wires and a second wire of the plurality of  
11 wires, said second wire already tri-stated or can be tri-stated, said wire pair having a same-  
12 direction switching probability  $\phi_{SD}$  per clock cycle that is no less than a pre-selected minimum  
13 same-direction switching probability  $\phi_{SD,MIN}$  or having an opposite-direction switching  
14 probability  $\phi_{OD}$  per clock cycle that is no less than a pre-selected minimum opposite-direction  
15 switching probability  $\phi_{OD,MIN}$ , said first wire and said second wire satisfying at least one  
16 mathematical relationship, said at least one mathematical relationship involving  $L_{COMMON}$  and  
17  $W_{SPACING}$ , said  $W_{SPACING}$  defined as a spacing between the first wire and the second wire, said  
18  $L_{COMMON}$  defined as a common run length of the first wire and the second wire.

1 41. The computer system of claim 40, said at least one mathematical relationship comprising:

2  $W_{SPACING}$  no greater than a pre-selected minimum spacing  $W_{SPACING, MAX}$ ; and

3  $L_{\text{COMMON}}$  no less than a pre-selected minimum common run length  $L_{\text{COMMON, MIN}}$ .

1 42. The computer system of claim 40, said at least one mathematical relationship comprising  $F_{\text{LW}}$   
2  $\geq F_{\text{LW, MIN}}$ , said  $F_{\text{LW}}$  defined as  $L_{\text{COMMON}}/W_{\text{SPACING}}$ , said  $F_{\text{LW, MIN}}$  defined as a pre-selected minimum  
3 value of  $F_{\text{LW}}$ .

1 43. The computer system of claim 40, wherein said algorithm identifying at least one wire pair  
2 includes:

3 said algorithm identifying at least one high-power wire; and

4 for a high-power wire of the at least one high-power wire, said algorithm identifying a  
5 good neighbor wire of the high-power wire, wherein the first wire of the wire pair is the high-  
6 power wire, and wherein the second wire of the wire pair is the good neighbor wire.

1 44. The computer system of claim 40, wherein if said algorithm determines that said second wire  
2 is not already tri-stated but can be tri-stated, then further comprising said algorithm adding tri-  
3 stating logic to the second wire.

1 45. The computer system of claim 40, wherein if said algorithm determines that  $\phi_{\text{OD}}$  is no less  
2 than  $\phi_{\text{OD, MIN}}$ , then further comprising said algorithm adding logic for inverting the second wire  
3 along the common run length.

1 46. The computer system of claim 40, further comprising the computer algorithm adding  
2 blocking logic for blocking propagation of a signal from the second wire while the second wire is  
3 tri-stated.

1 47. The computer system of claim 40, further comprising the computer algorithm reducing  
2  $W_{\text{SPACING}}$ .

1 48. The computer system of claim 40, wherein if said the computer algorithm identifies the at  
2 least one wire pair as including a plurality of wire pairs, then further comprising:

3       said computer algorithm ranking the wire pairs in accordance with power dissipation  
4 savings;

5       said computer algorithm developing a list of the ranked wire pairs in sorted order of the  
6 power dissipation savings; and

7       said computer algorithm truncating the list at a point of diminishing returns in the power  
8 dissipation savings, in accordance with a predetermined truncation criterion.

1 49. The computer system of claim 40, wherein  $W_{\text{SPACING}}$  is a predetermined spacing, and wherein  
2  $L_{\text{COMMON}}$  is a predetermined common run length.

1 50. The computer system of claim 40, wherein  $W_{\text{SPACING}}$  is an established spacing, and wherein  
2  $L_{\text{COMMON}}$  is an established common run length.

1 51. A computer program product, comprising: a computer usable medium having a computer  
2 readable program code embodied therein for designing an electrical wiring structure having a  
3 plurality of wires, wherein the computer readable program code includes an algorithm, said  
4 algorithm identifying at least one wire pair, said wire pair including a first wire of the plurality of  
5 wires and a second wire of the plurality of wires, said second wire already tri-stated or can be tri-  
6 stated, said wire pair having a same-direction switching probability  $\phi_{SD}$  per clock cycle that is no  
7 less than a pre-selected minimum same-direction switching probability  $\phi_{SD,MIN}$  or having an  
8 opposite-direction switching probability  $\phi_{OD}$  per clock cycle that is no less than a pre-selected  
9 minimum opposite-direction switching probability  $\phi_{OD,MIN}$ , said first wire and said second wire  
10 satisfying at least one mathematical relationship, said at least one mathematical relationship  
11 involving  $L_{COMMON}$  and  $W_{SPACING}$ , said  $W_{SPACING}$  defined as a spacing between the first wire and  
12 the second wire, said  $L_{COMMON}$  defined as a common run length of the first wire and the second  
13 wire.

52. The computer program product of claim 51, said at least one mathematical relationship  
comprising:

$W_{SPACING}$  no greater than a pre-selected minimum spacing  $W_{SPACING,MAX}$ ; and

$L_{COMMON}$  no less than a pre-selected minimum common run length  $L_{COMMON,MIN}$ .

1 53. The computer program product of claim 51, said at least one mathematical relationship  
2 comprising  $F_{LW} \geq F_{LW,MIN}$ , said  $F_{LW}$  defined as  $L_{COMMON}/W_{SPACING}$ , said  $F_{LW,MIN}$  defined as a pre-

1 selected minimum value of  $F_{LW}$ .

1 54. The computer program product of claim 51, wherein said algorithm identifying at least one  
2 wire pair includes:

3 said algorithm identifying at least one high-power wire; and

4 for a high-power wire of the at least one high-power wire, said algorithm identifying a  
5 good neighbor wire of the high-power wire, wherein the first wire of the wire pair is the high-  
6 power wire, and wherein the second wire of the wire pair is the good neighbor wire.

1 55. The computer program product of claim 51, wherein if said algorithm determines that said  
2 second wire is not already tri-stated but can be tri-stated, then further comprising said algorithm  
3 adding tri-stating logic to the second wire.

1 56. The computer program product of claim 51, wherein if said algorithm determines that  $\phi_{OD}$  is  
2 no less than  $\phi_{OD,MIN}$ , then further comprising said algorithm adding logic for inverting the second  
3 wire along the common run length.

1 57. The computer program product of claim 51, further comprising the computer algorithm  
2 adding blocking logic for blocking propagation of a signal from the second wire while the second  
3 wire is tri-stated.

1 58. The computer program product of claim 51, further comprising the computer algorithm  
2 reducing  $W_{\text{SPACING}}$ .

1 59. The computer program product of claim 51, wherein if said the computer algorithm identifies  
2 the at least one wire pair as including a plurality of wire pairs, then further comprising:

3 said computer algorithm ranking the wire pairs in accordance with power dissipation  
4 savings;

5 said computer algorithm developing a list of the ranked wire pairs in sorted order of the  
6 power dissipation savings; and

7 said computer algorithm truncating the list at a point of diminishing returns in the power  
8 dissipation savings, in accordance with a predetermined truncation criterion.

1 60. The computer program product of claim 51, wherein  $W_{\text{SPACING}}$  is a predetermined spacing,  
2 and wherein  $L_{\text{COMMON}}$  is a predetermined common run length.

1 61. The computer program product of claim 51, wherein  $W_{\text{SPACING}}$  is an established spacing, and  
wherein  $L_{\text{COMMON}}$  is an established common run length.